TECHNICAL NOTICE SMTS

SMTS-* Modules

NTTS-0323

Vizimax, 2284 de la Province Street
Longueuil (Quebec), Canada, J4G 1G1
Tél: (450) 679-0003 Fax: (450) 679-9051 www.vizimax.com

TECHNICAL NOTICE

STATIC TIME

DELAY RELAYS

SMTS

NTTS-323 REV. 0

Snemo ltée/Ltd, 3605 Isabelle, Brossard (Québec), Canada, J4Y-2R2
Tél. : (514)-444-3001, Mtl : (514)-861-7102, Fax : (514)-444-3009

Static time delay relays SMTS

General information

AUTHOR :	Robert Desvigne	93-03-01
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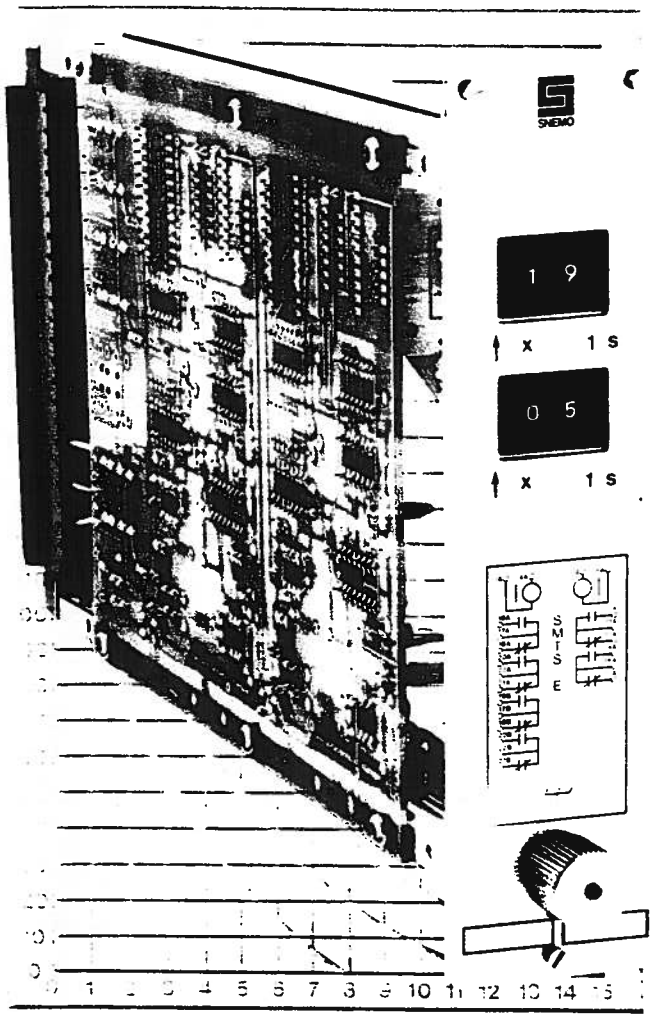
Revision history

DATE	REV.	DESCRIPTION	AUTHOR	VERIFIED	APP.
96-12-19	**0**	**First release**	R.D.		

Static time delay relays

SMTS

FCTS-102



Snemo static time delay relays, part of the Versa® series, are designed to provide timing functions for all electrical automatic control device applications.

- Standard module : 1 seat
- Adaptable for the Versa® rack (ref : 01-001)
- 1 to 4 time-delay circuits
- 6 time ranges available from 10 ms to 9.9 hours
- 8 available configurations
- Versa® rack door or transparent, sealable protective cover

Principle of operation

SMTS relays generate their own pulses from individual RC oscillators on each circuit.

The circuit(s) can be adapted as needed for "E" (pick up) or "D" (drop out) mode when ordered.

"E" mode delays the closing of contacts when a command signal is applied.

"D" mode delays the closing of contacts when a command signal disappears.

The time-delay is selected from the front with a two-digit digital encoding device that offers a 100-point resolution, depending on the time-delay range specified when ordered.

It can be useful to have short-circuiters on configurations A,B and C for module removal operations in applications with sustained continuity of operation.

General Specifications

Snemo

3605, rue Isabelle, Brossard (Québec) Canada J4Y 2R2
Tél.: (514) 444-3001 • Fax: (514) 444-3009

Technical Characteristics

Features	SMTS
Power supply	129 VDC (1)
Range of use	105 to 141 VDC
Contact capacity	5 Amp.
Typical relay consumption de-energized (2)	0.5 W
Typical relay consumption energized (2)	1.75 W
Consumption at input start-up (2)	1.25 W
Minimum time reset, E mode	8.0 msec
Minimum start-up time, D mode	8.0 msec
Insulation test voltage 1 minute	1500 V
Precision of operating delay	+/− 2% + ε with 6< ε <25 msec

(1) Available at 24 VDC (please consult SNEMO for any other voltage).
(2) Typical consumption at 129 VDC.

Available configurations

Type	Circuit number	SPDT	Maximum number of short circuiters
A	1	2	4
B	1	4	4
C	2	2	4
D	2	4	•
E	2	1×4 & 1×2	•
F	3	2	•
G	3	1×4 & 2×2	•
H	4	2	•

Available Time Delays

Time scales	Increment	Time range
V	10 msec	0 to .99 sec
W	0.1 sec	0 to 9.9 sec
X	1.0 sec	0 to 99 sec
Y	10 sec	0 to 990 sec
Z	1.0 min	0 to 99 min
L	0.1 hour	.1 to 9.9 hours

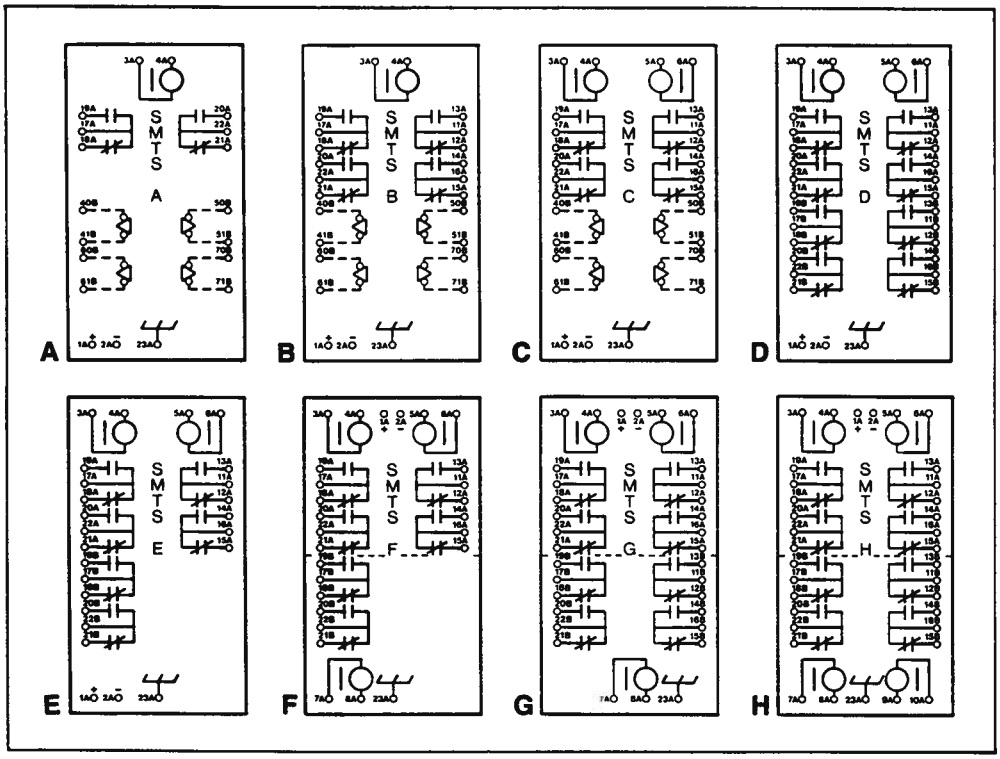
Codification

1. Configuration type (A to H)
2. Number of short-circuiters — 1 to 4 (on A,B,C only)
3. E or D of 1st circuit
4. Time scale of 1st circuit
5. E or D of 2nd circuit
6. Time scale of 2nd circuit
7. E or D of 3rd circuit
8. Time scale of 3rd circuit
9. E or D of 4th circuit
10. Time scale on 4th circuit

Example :

	1	2	3/4	5/6	7/8	9/10
SMTS	A	4	E/X	•	•	•
SMTS	C	0	D/X	E/W	•	•
SMTS	H	0	D/Y	E/V	D/Z	D/L

Connection Diagram



SMTS

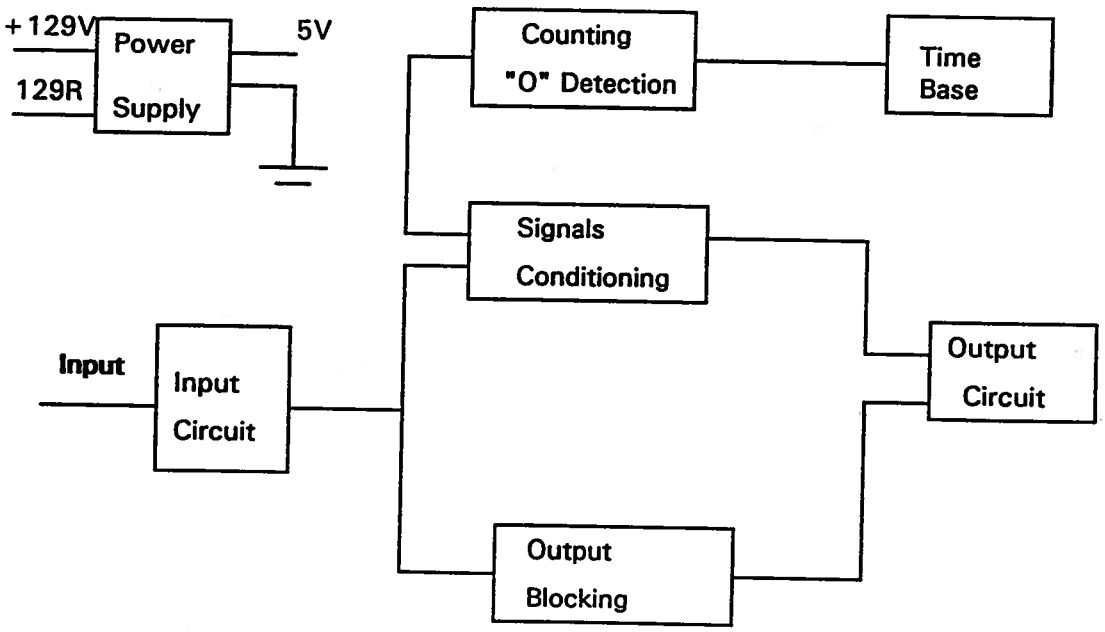
OPERATION

Each module can contain up to 5 PCBs, one for the output relay and auxiliary power supply, the rest (max. four) being time delay circuits.

SMTS As is a special version of SMTS. It has only 3 PCBs:

- Time delay circuit
- Output relays and aux. power supply circuit.
- Lowering of entry circuit impedance circuit

Block diagram:



1. Power Supply Circuit

It has two parts

The first, common to all time-delayed circuits of the same module is located on the PCB of the output relays. It has a protection against transient voltage surcharges (VR1) and a rectifying bridge (DB1). The purpose of the rectifier is to insure a proper functioning of the time-delayed circuits even when the polarity of DC power supply is reversed.

The second part is located on each of the time-delayed circuits and has the purpose of lowering the voltage of the auxiliary supply to a level acceptable by the integrated circuit (5v) this part of the circuit is composed by a Zener diode (DZ1), a resistor (R6) and a capacitor (C9).

The maximum current, usable at 5V is:

Auxiliary power supply at 129v.

$$I = \frac{Vin\ (min) - Vdz}{R6} = \frac{105-5.6}{39K} = 2.5mA$$

Auxiliary power supply at 24V

$$I = \frac{Vin\ (min) - Vdz}{R6} = \frac{19.2 - 5.2}{5.6K} = 2.5\ mA$$

2. Input Circuit

The input circuit is composed by a protection against transient voltage surcharges (VR1), a rectifying bridge (DB1), a resistor limiting the current (R8), a smothing capacitor (C10), a Zener diode (DZ2) to prevent tripping under an accepted threshold and an opto-coupler (U9).

The opto-coupler allows a galvanic isolation between the input signal and the auxiliary supply. The resistor (R8) has the role of lowering the impedance of the input circuit.

Whenever a signal having a higher amplitude than the value of Zener diode (DZ2) is applied on the entry terminals, the DEL of the opto-coupler (U9) is polarizing the base of the transistor and is lowering the potential of the collector to the zero threshold.

The resistor (R5) on the transistor is collector helps to keep the potential of the collector at 5V, whenever there is not input signal (logic level 1).

The inverters (U7c) and (U7d) as well as the resistor (R3) and the capacitor (C5) act as anti-bouncing filter.

Therefore, at test point PT3 we will have 5V if there is no input signal and 0V when there is one.

3. Time Base Generating Circuit:

This circuit generates pulses for the programmable counter. It is made out of an oscillator (U8), components fixing the frequency of the oscillations (RV1, R4 and C6) and a divider with multiple stages (U6).

The function of this divider is to allow the oscillator to work in a frequency range where it is most stable, no matter the range of time delay required.

The working frequency of the oscillator is determined by choosing the capacitor (C6) and the resistor (R4).

The potentiometer(RV1) allows an accurate adjustment of the frequency.

In case of very long time delays (ranges Y,Z, and L) the impulses are divided by 512 (2^9) by (U6).

You will find in section (XX) a table indicating the impulses periodes at the level of test points PT1 and PT2, the position of the divider, the values of (R4) and (C6) as well as the exact resistance of the potentiometer (RV1) acording to the required range.

4. Signals conditionning circuit acording to "E" or "R"

The logic gate "OR" exclusif "(U5)", allows the conditioning (inverting or not) of various logic signals in order to observe the functionning of the two operation modes:

E -pick up

R -drop out

When the operating mode is "E" ,the input signal (PT3) is not inverted by (U5b) but by the (U5d). Therefore, when an input signal is present (PT3=0V), and this signal is inverted by (U5d) the controle of the programmable counter is at 1 (counting operation). The output signal of the multiplexer is not inverted by (U5a) either.

When the operating mode is "R" the input signal (PT3) is inverted a first time by U5b and inverted again into its original status by U5d. Therefore, whenever the input signal is present (PT3=0V) and this signal is inverted twice we retrive the control signal of the programmable counter at the 0 logic level (zero reset of the counter). The output signal of the multiplexer is also inverted by (U5a).

5. Counting and Rapid Detection of "00" Circuit.

The counting circuit determins the duration of time-delay operation.

It is made out of two digital encorders (placed on the front plate of the module) loading resistors (RD1) a programmable counter (U2), a code detector "00" on the display and a multiplexer.

The programmable counter first divides by 100 the pluses received on the pin 1 (input connection 3,4,5,6,19,20,21,22 on 0 level logic), than counts these pulses unitl their number matches the number indicated by the two digital encorders. When this occurs, the logic level on the pin 23 changes its logic status from 0 to 1.

The signal received on the pin 13 allows either the zero reset (o status) or the counting operation (1 status). the circuit (U1) allows the fast detection of the displaying code "00". Whenever the two digital encoders are reset at zero, the output of (U1) change into logic level "1" (test point PT4). This signal triggers the multiplexer which in turn decides if the signal which will activate the output relay will come from the programmable counter or will be a direct consequence of the input signal.

6. Output Blocking Circuit

This circuit has the role of blocking any output signal as long as no input signal was applied, once the module is voltage fed.

The circuit is a bistable type "SET/RESET". When the voltage is fed and as long as the capacitor (C3) did not change at logic status "1" through the resistor (R1), the output of (U3a) is at logic status "1".

When the capacitor (C3) is charged , the bistable maintains the status of (U3a) until an input signal is applied (PT3="0"). Then the bistable changes its status and stays in the logic status "1" until the voltage feed is lost.

the gate (U3d) inverts the signal present on (U3a) and conditions the output circuit.

7. Output Circuit

The function of this circuit is to activate an output relay according to the ouptut status of the multiplexer, if whenever and only the signal for blocking the output (U3d pin 11) is at the logic level "1".

If the output relay is activated the test point (PT5) is at logic status "0". If the relay is not activated the test point (PT5) will be at logic status "1".

SMTS

STATIC TIMING RELAY

1- DESCRIPTION OF SETTINGS

1.1 EXTERNAL SETTINGS

For each timing circuit of this relay, a numerical encoding switch is located on the front panel. These encoders indicate and switches the multiplying factor of the time base. Under each encoders, the time base and the operation mode are also indicated (↑ CLOSE or ↓ TRIP).

1.2 ADJUSTMENT METHOD AND INFLUENCE

Each digit has two buttons : depressing the top button of the corresponding digit raises the setting by one increment each time and depressing the lower digit lowers the setting by one, each time. In reference to FIGURE 1, switch setting will change timing operation and is dependent on the time scale.

1.3 INTERNAL SETTINGS

For each timing circuit in the relay, there is only one adjustement, trimming potentiometer RV1, used to precisely adjust the period associated with the time base selected.

1.4 TIME PERIOD

In order to change the time period of the relay, resistor R4 and capacitor C6 have to be changed.

TYPE	PERIOD MIN (mS)	PERIOD TYPICAL (mS)	PERIOD MAX (mS)
V	0,099	0,100	0,101
W	0,990	1,000	1,010
X	9,900	10,000	10,100
Y	0,193	0,195	0,197
Z	1,160	1,172	1,184
L	6,960	7,030	7,100

FIGURE 1

2 PERFORMANCE VERIFICATION AND ADJUSTEMENTS

2.1 EQUIPEMENT REQUIRED

- Doble F2000 series test bench, or equivalent
- Auxiliairy supply source,0-129Vdc ± 20%
- Voltmeter, 0-300 Vdc ±1%
- Frequency meter, 0-12 mS, ±0.1%

2.2 TEST SETUP

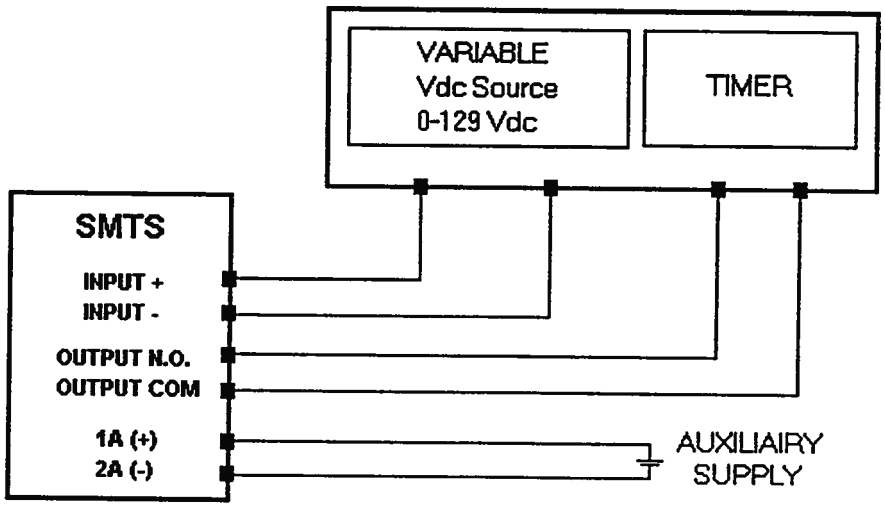


FIGURE 2

2.3 TEST PROCEDURES

Adjust each encoder switch on relay front panel to obtain desired timing and period as per FIGURE 1

Apply nominal operating voltage to relay under test (+ on terminal 1A, - on terminal 2A)

For each timing input, proceed as follows :

Connect N.O. and common to timer input
Apply nominal power to respective input

FOR ↑ CLOSE ("E" MODE)

Measure time between input signal application and closing of related output contacts

FOR ↓ TRIP ("R" MODE)

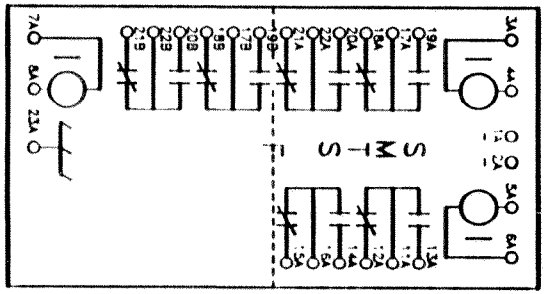
Measure time between removing of input signal and opening of associated output contacts

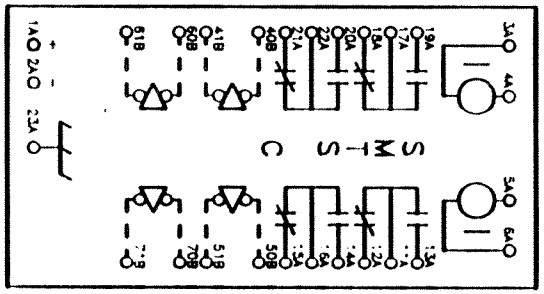
Compare obtained timing values with corresponding values in FIGURE 3 . These values must be within MIN and MAX corresponding to selected time scale.

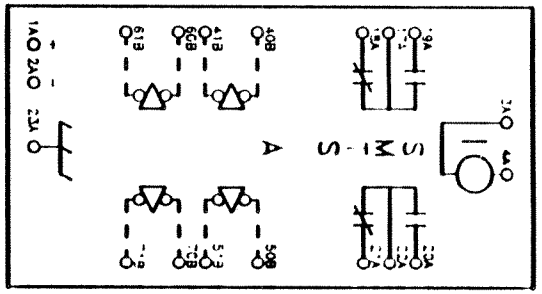
TIME SCALE	SWITCH SETTING	MIN TIME	MAX TIME
V	01	114 mS	131 mS
W	01	1.09 S	1.13S
X	10	10.89 S	11.13 S
Y	10	108.9 S	111.12 S
Z	10	653.4 S	666.62 S
Y	01	3920 S	4000 S

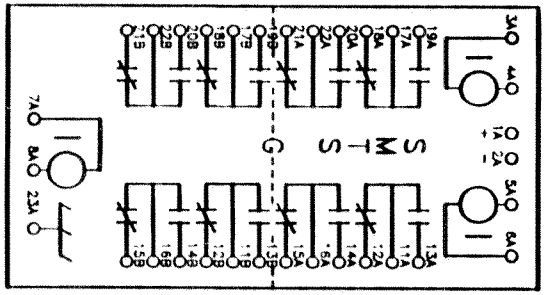
FIGURE 3

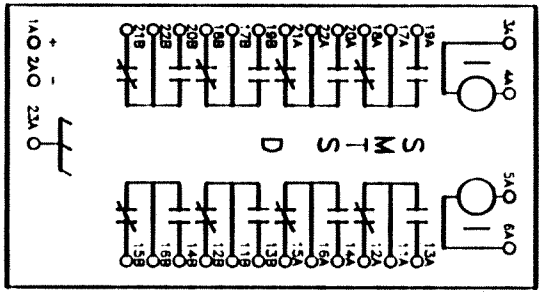
FEUILLE SHEET 1 DE OF 1 No P,B,T,S 1,0,2 B

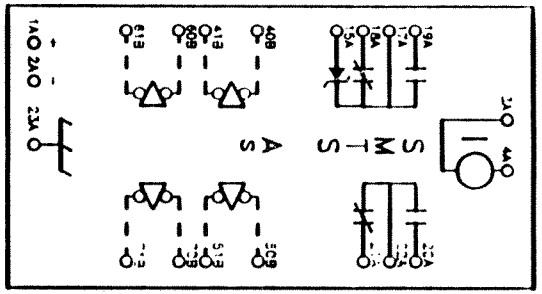


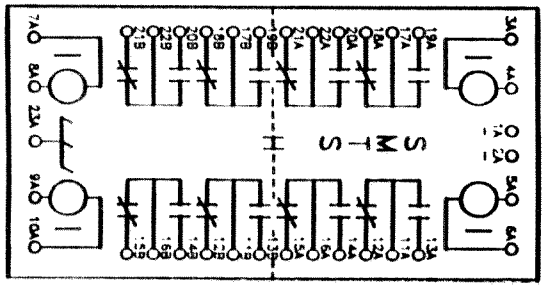


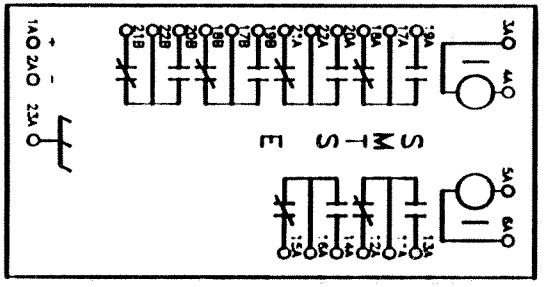


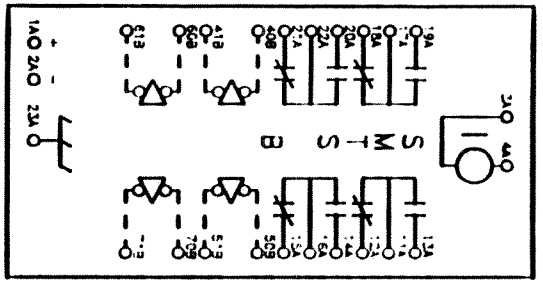












IND	DATE AAMJ/YMD	REVISIONS	DES. DRA.	VER. CHE.	APP.
B	93-10-26	STANDARDISATION DU DESSIN ET SMTS-Aa MODIFIE (DIODE ZENER).	E.A.		
A	89-07-24	AJOUT DU SMTS Aa.	Y.M.	S.D.	MMB

SCEAU SEAL

FORMAT: A3

ECHELLE: SCALE: N/A

DATE: AAMJ/YMD	87-08-28
DESSINE DRAWN	Y. MASSE
PROJETE PROJECTED	N/D
VERIFIE CHECKED	S. DESBOIS
APPROUVE APPROVED	M.MONT-BRIANT
DOSSIER: FILE:	
REFERENCE:	

Snemo Ltee/Ltd

MODULE SMTS *

PLAN DE BORNAGE

FEUILLE SHEET 1 DE OF 1 No P,B,T,S 1,0,2 B